WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising a plurality of semiconductor devices formed on a substrate,

wherein a principal plane of said substrate is partitioned into a plurality of device regions and into a plurality of routing regions each crossing a boundary between said plurality of device regions,

a device group including one or more semiconductor devices among said plurality of semiconductor devices and a local interconnect for connecting said semiconductor devices included in said device group are disposed within said plurality of device regions, and

a global routing for connecting said device groups to each other is disposed within said plurality of routing regions.

2. A semiconductor integrated circuit device comprising a plurality of semiconductor devices formed on a substrate,

wherein a principal plane of said substrate is partitioned into a plurality of device regions having one shape and two-dimensionally arranged in a repetitive cycle corresponding to said shape and into a plurality of routing regions having said shape and two-dimensionally arranged in said repetitive cycle corresponding to said shape to be shifted from said plurality of device regions by a distance,

a device group including one or more semiconductor

devices among said plurality of semiconductor devices and a local interconnect for connecting said semiconductor devices included in said device group are disposed within said plurality of device regions, and

a global routing for connecting said device groups to each other is disposed within said plurality of routing regions.

3. The semiconductor integrated circuit device of Claim 1 or 2,

wherein a routing terminal crossing a boundary between said plurality of routing regions is disposed within at least one of said plurality of device regions.

4. The semiconductor integrated circuit device of Claim 2,

wherein said distance is a half of said repetitive cycle.

5. An exposure method comprising the steps of:

forming a lower layer pattern on a substrate to be exposed by successively forming a corresponding pattern in each of a plurality of first regions obtained by partitioning a principal plane of said substrate to be exposed through exposure using electromagnetic waves or a charged particle beam; and

forming an upper layer pattern over said lower layer pattern on said substrate to be exposed by successively

forming a corresponding pattern in each of a plurality of second regions obtained by partitioning the principal plane of said substrate to be exposed through the exposure using electromagnetic waves or a charged particle beam,

wherein each of said plurality of second regions crosses a boundary between said plurality of first regions.

6. An exposure method comprising the steps of:

forming a lower layer pattern on a substrate to be exposed by successively forming a corresponding pattern in each of a plurality of first regions obtained by partitioning a principal plane of said substrate to be exposed through exposure using electromagnetic waves or a charged particle beam; and

forming an upper layer pattern over said lower layer pattern on said substrate to be exposed by successively forming a corresponding pattern in each of a plurality of second regions obtained by partitioning the principal plane of said substrate to be exposed through the exposure using electromagnetic waves or a charged particle beam,

wherein said plurality of first regions are in one shape and two-dimensionally arranged in a repetitive cycle corresponding to said shape, and

said plurality of second regions are in said shape and two-dimensionally arranged in said repetitive cycle corresponding to said shape to be shifted from said plurality

of first regions by a distance.